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(54) Process for manufacturing electronic devices comprising non-volatile memory cells

(57) The process for the manufacturing electronic devices including memory cells (72) comprises the steps of: forming, on a substrate (2) of semiconductor material, multilayer stacks (54) including a floating gate region (40a), an intermediate dielectric region (41a), and a control gate region (50a); forming a protective layer (75) extending on top of the substrate (2) and between the multilayer stacks (54) and having a height at least equal to the multilayer stacks. The step of forming multilayer stacks (54) comprises the step of defining the control gate region (50a) on all sides so that each control gate region is completely separate from adjacent control gate regions. The protective layer (75) isolates the multilayer stacks (54) from each other at the sides. Word lines (80a) of metal extend above the protective layer (75) and are in electrical contact with the gate regions.

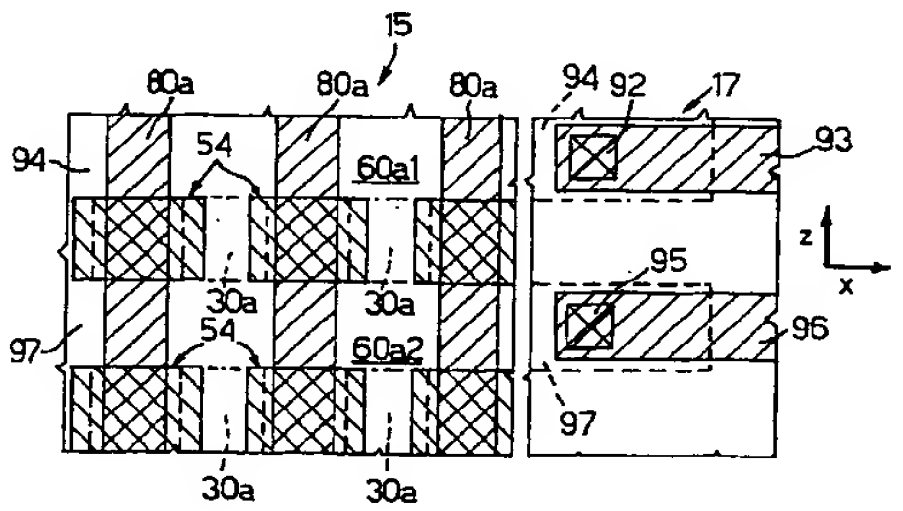

Fig. 23

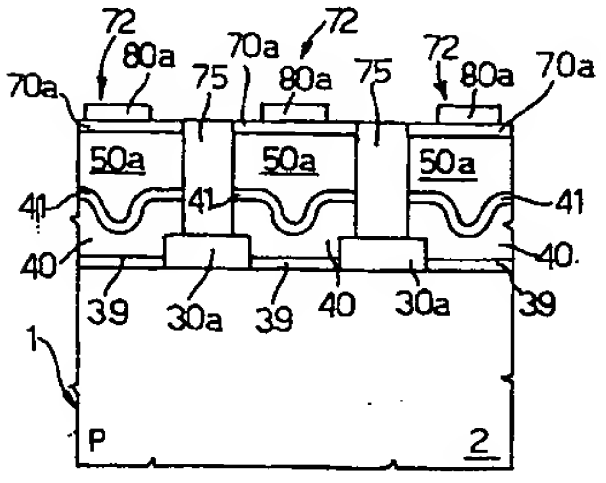

Fig. 22

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Description

[0001] The present invention regards a process for manufacturing electronic devices comprising nonvolatile memory cells of reduced dimensions.

[0002] Devices using nonvolatile memories, for example of the EPROM type or EEPROM type, such as smart cards, complex microcontrollers and mass storage devices which require programmability of the individual byte, call for increasingly higher levels of performance and reliability.

[0003] In practice, from the technological standpoint, this means that it is necessary to get high performances (i.e., increasingly thinner tunnel oxides, ever more reduced programming voltages, increasingly greater cell current-driving capability, etc.) to coexist with an extremely high reliability: one hundred thousand programming cycles and retention of the stored charge for at least ten years are by now considered the minimum requisites for accepting these products on the market.

[0004] Therefore, it is necessary to develop new manufacturing processes and new geometries that are able to eliminate some of the critical aspects typical of memories, thus increasing their intrinsic reliability without reducing their performance, both for "embedded" applications (i.e., ones in which the memory cells are associated to electronic devices that perform preset functions) and for stand-alone applications (i.e., ones in which the device is merely a nonvolatile memory).

[0005] In particular, the reduction in the dimensions of memory devices entails severe constraints as regards formation of contacts and alignment of contacts with the drain regions.

[0006] For reducing the dimensions of memory devices, alternate metal ground (AMG) devices are known, wherein the diffused source lines and diffused drain lines are parallel, and the contacts are formed outside the area of the memory cells.

[0007] However, these memory devices have the problem that the word lines, formed by non-planar polysilicon strips defining the control gate regions of the memory cells, undergo sharp changes in direction in reduced spaces (corresponding to the width of the diffused source and drain lines). In addition, the polysilicon strips are not well insulated from the substrate because of the reduced thickness of the tunnel layer that is present there.

[0008] The aim of the present invention is to provide a manufacturing process allowing reduction of the constraints as regards formation and alignment of the contacts of the memory cells, and hence reduction of the dimensions of the memory cells without reducing their performance.

[0009] According to the present invention, a process for manufacturing electronic devices comprising nonvolatile memory cells, and an electronic device comprising nonvolatile memory cells are provided, as defined in Claim 1 and Claim 13, respectively.

[0010] For a better understanding of the present invention, a preferred embodiment thereof will now be described, as a non-limiting example, with reference to the attached drawings, wherein:

- Figure 1 shows a cross-section through a wafer in an initial step of the manufacturing process according to the invention;
- Figures 2-8 show cross-sections similar to that of Figure 1, in subsequent manufacturing steps;
- Figure 9 shows a top view of the wafer of Figure 8;
- Figure 10 shows a cross-section similar to that of Figure 8, in a subsequent manufacturing step;
- Figure 11 presents a top view of one part of the wafer of Figure 10;
- Figure 12 shows a cross-sectional view of the wafer, taken along plane XII-XII of Figure 10, in a subsequent manufacturing step;
- Figure 13 shows a cross-section similar to that of Figure 12, taken along a different portion of the electronic device, in a subsequent manufacturing step;
- Figure 14 shows a cross-section similar to that of Figure 12, in a subsequent manufacturing step;
- Figure 15 shows a cross-section similar to that of Figure 13, in a subsequent manufacturing step;
- Figure 16 shows a cross-section similar to that of Figure 14, in a subsequent manufacturing step;
- Figure 17 shows a cross-section similar to that of Figure 15, in a subsequent manufacturing step;
- Figure 18 shows a cross-section similar to that of Figure 16, in a subsequent manufacturing step;
- Figure 19 shows a cross-section similar to that of Figure 17, in a subsequent manufacturing step;
- Figure 20 shows a cross-section similar to that of Figure 18, in a subsequent manufacturing step;
- Figure 21 shows a cross-section similar to that of Figure 19, in a subsequent manufacturing step;
- Figure 22 shows a cross-section taken along plane XXII-XXII of Figure 20, in a subsequent manufacturing step;
- Figure 23 shows a top view of the wafer of Figure 22; and
- Figure 24 shows an equivalent electrical circuit of a memory device according to the present invention.

[0011] The following description regards an embodiment of a device containing EPROM memory cells and transistors. The invention is not, however, limited to EPROM memories, but may be applied to memories of a different type, such as flash-EEPROM and EEPROM memories, possibly with suitable adaptations to take into account the specific geometries of the memory cells.

[0012] In a per se known manner, the memory cells form a memory array and are formed in a wafer part, hereinafter also referred to as matrix area 15, while the

transistors are formed in a wafer, hereinafter also referred to as circuitry area 16.

[0013] In Figure 1, a wafer 1 formed by a monocrystalline silicon substrate 2, here of a P type, has undergone the steps of definition of the active areas.

[0014] In detail, on the surface 3 of the substrate 2 is formed a double layer of silicon oxide 8 and silicon nitride 12.

[0015] The matrix area 15 defines a grid, partly shown in Figure 1; Figure 1 moreover shows a part of the circuitry area 15 in which LDD-type NMOS transistors will be formed, in the considered example.

[0016] Further areas may be provided for further electronic components, not shown in the drawings.

[0017] In the matrix area 15, strips of the wafer 1 which are parallel to one another and perpendicular to the plane shown in Figure 1, are covered by a first isolation mask 20 of resist. In addition, in the circuitry area 16, regions corresponding to the active areas are covered by the first isolation mask 20.

[0018] As shown in Figure 2, by means of the first isolation mask 20 the nitride layer 12 and oxide layer 8 are anisotropically etched. The remaining portions of the nitride layer 12 and oxide layer 8 form a hard mask having elongated openings 21a in the form of strips in the matrix area 15 and openings 21b in the circuitry area 16.

[0019] Next, a second isolation mask 25 of resist is formed and entirely covers the matrix area 15, leaving the circuitry area 16 uncovered.

[0020] Subsequently, the substrate 2 is etched at the openings 21b in the circuitry area 16 where uncovered by the first isolation mask 20 and by the hard mask 12, 8, so as to form trenches 28 (Figure 2). Then the first isolation mask 20 and second isolation mask 25 are removed, and the free surface of the substrate 2 is cleaned from any impurities.

[0021] Alternatively, it is possible to etch the hard mask 12 and then remove the first isolation mask 20, before depositing the second isolation mask 25.

[0022] Next, the substrate 2 is etched in the circuitry area 16 where the latter is not protected by the hard mask 12, 8, so as to form trenches 28.

[0023] Subsequently, possibly a first thermal oxidation is carried out at a high temperature, and then a second oxidation is performed for relieving the possible stress induced in the wafer 1 when the trenches 28.

[0024] Subsequently, for example using CVD techniques, an oxide layer 30 is deposited which fills the trenches 28 and openings 21a, as shown in Figure 3, until also the nitride portions 12 are covered. The oxide layer 30 can be formed also from a multilayer.

[0025] Subsequently, the wafer 1 is planarized using the CMP technique. During this step, the oxide layer 30 is removed everywhere above the level of the nitride portions 12. Next, also the nitride portions 12 and the portions of the oxide layer 30 comprised between them are partially removed differently in the circuitry area 16 and in the matrix area 15. In fact, since the nitride portions 12 are set further apart in the circuitry area 16 than in the matrix area 15, the height of the remaining nitride portions 12 and oxide portions 30 is smaller in the circuitry area 16 than in the matrix area 15.

[0026] Using a further resist mask (not shown) which covers the matrix area 15, it is optionally possible to further partially remove the oxide layer 30 in the circuitry area 16, to increase the difference in height with respect to the matrix area 15. Consequently, first field oxide regions 30a are formed in the matrix area 15, and second field oxide regions 30b are formed in the circuitry area 16; the second field oxide regions 30b having a smaller height than the first field oxide regions 30a, as shown in Figure 4. The first field oxide regions 30a have the shape of strips extending perpendicularly with respect to the drawing, corresponding to the shape of the openings 21a of Figure 2.

[0027] Subsequently, the nitride portions 12 are removed completely using phosphoric acid at a high temperature, and a sacrificial oxide layer 38 is grown either after the oxide portions 8 have been removed or directly on the oxide portions 8 themselves to protect the substrate 2 during the subsequent steps, as shown in Figure 4.

[0028] A threshold implant is then carried out to modify the voltage threshold of the transistors. The sacrificial oxide layer 38 is removed in the matrix area 15, and a tunnel oxide layer 39 is grown. A first polysilicon layer (poly1 layer 40) is deposited, which is to form the floating gate regions of the memory cells in the matrix area 15, and an interpoly dielectric layer 41 is formed, for example comprising a triple layer of silicon oxide/silicon nitride/silicon oxide (ONO layer).

[0029] Subsequently, a mask 45 is formed and covers the matrix area 15. Then the interpoly dielectric layer 41, the poly1 layer 40 and the tunnel oxide layer 39 are removed from the circuitry area 16 together with the sacrificial oxide layer 38. In this way, the structure shown in Figure 5 is obtained.

[0030] Next, the mask 45 is removed from the matrix area (Figure 6), and a gate oxide layer 46 is subsequently grown on the circuitry area 16, while the matrix area 15 is protected by the interpoly dielectric layer 41. A second polysilicon layer (poly2 layer 50) is deposited, which is to form the control gate regions of the memory cells (Figure 7).

[0031] Optionally, the wafer 1 may be planarized again using the CMP technique to obtain a planar profile of the surface of the poly2 layer 50. At the end, a small difference of level exists between the top surface of the poly2 layer 50 in the matrix area 15 and the top surface of the poly2 layer 50 in the circuitry area 16.

[0032] Subsequently (Figure 8), a first gate mask 51 is formed and covers the entire circuitry area 16 and, in the matrix area 15, defines first strips perpendicular to the sectional plane of Figure 8. Using the first gate

mask 51, the poly2 layer 50, the interpoly dielectric layer 41, and the poly1 layer 40 are etched and removed on top of the first oxide regions 30a so as to form centered elongated openings 52 having a smaller width than the field oxide regions 30a, as shown in Figure 9, where the edges of the field oxide regions 30a are indicated by dashed lines. The stack of layers 50, 41, and 40 is thus defined in one first direction (x direction).

[0033] Next (Figures 10-12) a second gate mask 55 is formed and covers the entire circuitry area 16 and, in the matrix area 15, defines second strips parallel to the sectional plane of Figure 10 (see in particular Figure 11). Subsequently, the stacks comprising poly2 layer 50, interpoly dielectric layer 41, poly1 layer 40, and tunnel oxide layer 39, as well as field oxide regions 30a, where these are not covered by the second gate mask 55, are etched and removed. The strips formed by layers 50, 41, 40 in the matrix area 15 are thus defined in a second direction (z direction) perpendicular to the first direction, thus forming stacks 54, each comprising a control gate region 50a, an interpoly dielectric region 41a, and a floating gate region 40a. The resulting structure in this step is shown in Figure 11, where the solid lines indicate the edges of the regions of the second gate mask 55 (highlighted by hatching with positive slope), the dashed lines indicate the edges of the stacks 54 in the z direction (the stacks being highlighted by hatching with negative slope), and the dashed-and-dotted lines indicate the first field oxide regions 30a.

[0034] Consequently, according to one aspect of the present invention, and as is evident from a comparison between Figures 10 and 12, the control gate regions 50a are delimited on all four sides along the directions x and z and are separate from the control gate regions 50a of the adjacent memory cells.

[0035] Subsequently (Figure 13), using a third gate mask 56 that covers the matrix area 15 completely (in a way not shown), as well as the portions of the poly2 layer 50 where the gate regions of the circuitry transistors are to be formed, the poly2 layer 50 is etched in the circuitry area 16. Consequently, the structure of Figure 13 is obtained, showing the circuitry area 16 where only one gate region 50b of a circuitry transistor is visible.

[0036] Next, the circuitry area 16 is masked, and the matrix area 15 is implanted by doping ionic species, in this case of the N type (S/D implant), in a known manner which, consequently, is not illustrated. Inside the substrate 2, on the two opposite sides of the stacks 54 where the first field oxide regions 30a are not present, N-type source regions 60a1 drain regions 60a are formed (Figure 14). Likewise, subsequently N-type and/or P-type doping ionic species are implanted in circuitry area 16 using a mask, so as to form LDD regions 60b, which are of the N-type in the example illustrated in Figure 15.

[0037] Next, a dielectric layer is deposited (for example TEOS - tetraethylorthosilicate). In a per se known manner, the TEOS layer undergoes an anisotropic etching, is removed completely from the horizontal portions and remains on the sides of the stacks 54 and of the gate regions 50b where it forms spacers 61a and 61b, respectively (Figures 14 and 15).

[0038] Subsequently (Figure 15), N-type and/or P-type doping ionic species are implanted in the circuitry area 16 using a mask to form source and drain regions 65b of the N^+ type and/or P^+ type, and thus more doped than the LDD regions 60b aligned to the spacers 61b.

[0039] Then a metallic suicide layer is formed (the metal typically being titanium, but also cobalt or any other transition metal) by depositing a metal layer over the entire surface of the wafer 1 and performing a heat treatment which causes the metal layer to react with the silicon (silicidation step). Subsequently, the non-reacted metal layer (for example the layer deposited on oxide regions) is etched away using an appropriate solution that leaves the metal silicide intact.

[0040] Silicidation causes the formation of silicide regions 70a in the matrix area 15 and 70b in the circuitry area 16, on top of the source and drain regions 65a, 65b and on top of the control gate regions 50a and gate regions 50b, as shown in Figures 16 and 17, wherein the memory cells thus obtained are designated by 72, and the circuitry transistor is designated by 73.

[0041] Then a protective layer 75 of dielectric material (or a number of dielectric material layers) is deposited, for example boron phosphorus silicon glass (BPSG), as shown in Figure 18 for the matrix area 15 and in Figure 19 for the circuitry area 16. The protective layer 75 covers the memory cells 72 completely in the matrix area 15 and the transistors 73 in the circuitry area 16. Then the structure is planarized, for example using the CMP technique. In particular, planarization is carried on as far as the silicide regions 70a on top of the control gate regions 50a of the memory cells 72 in the matrix area 15. Consequently, in the matrix area 15 the protective layer 75 remains only between the memory cells 72 (Figure 18). Because of the small height difference between the control gate regions 50a (and the corresponding suicide regions 70a) and the gate regions 50b (and the corresponding suicide regions 70b), in the circuitry area 16 the protective layer 75 remains also slightly above the gate regions 50b (Figure 19).

[0042] Finally, the contacts are formed. To this end, initially openings are formed in the protective layer 75. Then (Figure 20), a tungsten layer 77 is deposited having a thickness of approximately 800-1500 nm, using the known W-plug technology. Figure 20 shows, just to provide an example, an opening 78a extending throughout the thickness of the protective layer 75 as far as the surface of the substrate 2. The opening 78 is filled by the tungsten layer 77 so as to form a contact 77a for an N-type conductive region 79 formed in the substrate 2 and belonging to an electronic component (not shown). Likewise, as illustrated in Figure 21, above the gate regions 50b, in the circuitry area 16, openings 78b are formed that reach the silicide regions 70b on top of the

gate regions 50b. The openings 78b are filled with the tungsten layer 77 so as to form contacts 77b for the gate regions 50b.

[0043] A first interconnection level is then defined and exploits the tungsten layer 77 as if it were an aluminum standard metal layer. In particular, using a mask (not shown), selective portions of the tungsten layer 77 are removed on top of the protective layer 75. In the matrix area 15 word lines 80a are then formed perpendicular to the section plane of Figure 22, also visible in the top view of Figure 23, so as to connect together the control gate regions 50a of the memory cells 72 aligned on a same column (z direction in Figure 23). In this step, interconnection regions are moreover formed between the various components of the device, in particular between the matrix area 15 and the circuitry area 16 and between the transistors 73 (as well as between the other components, not shown, of the circuitry area 16).

[0044] The final structure of the matrix area 15 may be seen in Figures 22 and 23 and is shown schematically in Figure 24, which illustrates an array memory 91 comprising a plurality of cells 72 arranged in rows and columns. In detail, the control gate regions 50a of the memory cells 72 set vertically aligned (in a same column) are connected together by a respective word line 80a. The source regions 60a1 of the cells 72 comprise diffused source lines 94 extending within the substrate 2 and connected at one end to source contacts 92, which in turn are connected to a source metal line 93. The drain regions 60a2 of the cells 72 comprise diffused drain regions 97 (defining bit lines) extending within the substrate 2 and connected at one end to source contacts 95, which in turn are connected to drain metal lines 96. The source contacts 92 and drain contacts 95 are formed in an area 17 of the substrate 2 external to the matrix area 15. The source contacts 92 and drain contacts 95, as well as the source metal line 93 and drain metal lines 96, are altogether analogous to the contact 77a of Figure 20. Finally, Figure 24 shows selection transistors 98 and 99 connected to the source metal line 93 and, respectively, to the drain metal lines 96.

[0045] The described method makes allows a reduction in the dimensions of the memory cells because, as in the case of AMG cells, it is possible to form source contacts 92 and drain contacts 95 outside the matrix area 15, where the memory cells 72 are formed (area 17). In addition, the fact that the control gate regions 50a are completely separate from the control gate regions 50a of the adjacent cells in both directions by the protective layer 75, and that the word lines 80a comprise planar strips made of metallic material set apart from the substrate 2 by a distance equal to the height of the stacks 54 avoids the problems existing in AMG cells.

[0046] Furthermore, the process according to the invention reduces the dimensions of the memory matrix in a direction perpendicular to the word lines 80a. In fact, the use of a deposited field oxide, instead of a thermally grown field oxide, eliminates the presence of inclined oxide regions, usually referred to as birds beaks. In addition, since the diffused source lines 94 and diffused drain lines 97 are defined when etching poly2 layer 50, interpoly dielectric layer 41, poly1 layer 40, and tunnel oxide layer 39, as well as field oxide regions 30a, enables a more precise implantation as compared to known solutions.

[0047] Finally, it is clear that numerous modifications and variations can be made to the method and to the electronic device described and illustrated herein, all of which falling within the scope of the invention, as defined in the attached claims. For example, it is possible to implant the source/drain in the matrix area 15 before defining the gate regions of the transistors 73 in the circuitry area 16, exploiting the second gate mask 55 which covers the circuitry area 16. Furthermore, the silicidation step is optional. Finally, the sacrificial oxide 38 may be absent; in this case, the substrate 2 is protected during the threshold implantation step by the portion of the oxide layer 8 that remains after etching the nitride layer 12.

[0048] In addition, the contacts and interconnection lines may be formed using the so-called "damascene" technique, according to which, after depositing the protection layer 75, a stop layer, for example of silicon nitride, and then a further dielectric layer are deposited. With a second mask, the further dielectric layer is then etched. The etch terminates on the stop layer. Subsequently, using an appropriate mask, openings are formed in the protective layer 75, and then a tungsten layer is deposited having a thickness of approximately 800-1500 nm, using the known W-plug technology. Subsequently, the structure may be planarized to eliminate the excess tungsten.

[0049] Finally, the same process may be used to manufacture a different memory type, as mentioned previously. As regards flash memories and EPROM memories, the present process is particularly advantageous for technologies enabling body erasing, where the source region no longer requires a double implant and is formed during the drain implant, thus rendering the memory cells symmetrical. In the case of EEPROM memories, the process must of course be adapted so as to form selection transistors at the same time as memory transistors of the stacked type.

Claims

1. A process for manufacturing electronic devices including memory cells (72), comprising the steps of:

   on a substrate (2) of semiconductor material, forming stacks (54) including a floating gate region (40a) of semiconductor material, an intermediate dielectric region (41a), and a con-

trol gate region (50a) of semiconductor material;

forming a protective layer (75) of insulating material extending on top of said substrate and between said stacks, said protective layer (75) having a height at least equal to that of said stacks;

characterized in that said step of forming stack structures (54) comprises the step of defining said control gate region (50a) in two non-parallel directions so that each control gate region is separate and electrically insulated with respect to the control gate regions belonging to adjacent stack structures (54);

in that, during said step of forming a protective layer (75), said stack structures (54) are completely isolated with respect to one another in said two directions;

and in that it further comprises the step of forming word lines (80a) of conductive material which extend above said layer of insulating material and are in electrical contact with said control gate regions.

2. The process according to Claim 1, characterized in that said step of forming word lines (80a) comprises the steps of:

forming a conductive material layer (77) on top of said stack structures (54) and of said protective layer (75), said conductive material layer contacting said control gate regions (50a); and shaping said conductive material layer (77) to form said word lines (80a) and electrical interconnections (93, 96).

3. The process according to Claim 1 or 2, characterized in that said step of forming a protective layer (75) comprises the step of depositing an insulating material layer(75) and planarizing said insulating material layer level with said control gate regions (50a).

4. The process according to any of the foregoing claims, characterized by the step of forming conductive regions (50b, 79, 94, 97) on top of and within said substrate (2), and in that, after said step of forming a protective layer (75), the steps are carried out of forming openings (78a, 78b) in said protective layer (75), said openings extending from one surface of said protective layer (75) as far as said conductive regions (50b, 79, 94, 97), and of covering walls of said openings with said conductive material layer.

5. The process according to Claim 4, characterized in that said conductive material layer (77) is of tungsten.

6. The process according to any of the foregoing claims, characterized in that said step of forming stack structures (54) comprises the steps of:

- forming a composite layer comprising one first semiconductor material layer(40); a dielectric material layer (41) on top of said first semiconductor material layer; and a second semiconductor material layer (50) on top of said dielectric material layer;
- shaping said composite layer so as to form multilayer strips extending in one first of said two directions; and
- shaping said multilayer strips in one second of said two directions, said second direction being perpendicular to said first direction.

7. The process according to Claim 6, characterized in that before said step of forming stack structures (54) the steps are carried out of:

- forming at least one first insulating material layer (30) on top of said substrate (2); and
- defining said first insulating material layer so as to obtain insulating strips (30a) extending in said first direction on one first area (15) of said substrate;

and in that said step of shaping said multilayer strips in a second direction comprises selectively removing said insulating strips (30a) from substrate portions in said first area (15).

8. The process according to Claim 7, characterized in that, after said step of shaping said multilayer strips, a step is carried out of introducing doping ionic species into said substrate portions and forming diffused, elongated source and drain regions (94, 97) extending parallel to and alternating with one another.

9. The process according to Claim 8, further characterized by the step of forming contact regions (92, 95) across said protective layer (75) as far as ends of said diffused, elongated source and drain regions (94, 97), said contact regions (92, 95) extending externally to said first area (15).

10. The process according to any of Claims 7-9, characterized in that, before said step of forming insulating strips (30a) on said first area (15), the steps are carried out of making a hard mask (12) having openings (21a) on said first area (15), and forming trenches (28) in a second area (16) of said substrate (2) separate from said first area (15); in that said step of forming insulating strips (30a) comprises the steps of depositing a field material layer (30) filling said trenches (28) and said openings (21a), and of selectively removing said field mate-

rial layer (30) on top of said hard mask (12) and on top of said trenches (28) so as to simultaneously form said insulating strips (30a) on said first area (15) and insulating regions (30b) on said second area (16); said insulating strips (30a) in said first area (15) having a different height from said insulating regions (30b) in said second area (16).

11. The process according to Claim 10, characterized by the step of making electronic components (73) in said second area (16).

12. A process for manufacturing electronic devices, comprising the step of forming first insulating regions (30a) and second insulating regions (30b) in a first area (15) and, respectively, in a second area (16) separate from said first area (15), of a substrate (2) of semiconductor material, the process being characterized by the steps of:

- forming a hard mask (12) having openings (21a) on said first area (15);
- forming trenches (28) in said second area (16);
- depositing an insulating material layer (30) filling said trenches (28) and said openings (21a); and
- selectively removing said insulating material layer (30) on top of said hard mask (12) and on top of said trenches (28) so as to simultaneously form said first insulating regions (30a) and said second insulating regions (30b); said first insulating regions (30a) in said first area (15) having a different height from said second insulating regions (30b) in said second area (16).

13. An electronic device comprising:

- a substrate (2) of semiconductor material;
- memory cells (72), each including a stack (54) on top of said substrate; each of said stacks (54) comprising a floating gate region (40a) of semiconductor material, an intermediate dielectric region (41a), and a control gate region (50a) of semiconductor material; and
- a protective layer (75) extending on top of said substrate and between said stack structures (54), said protective layer having a height at least equal to that of said stack structures; and
- word lines (80a) of conductive material extending on top of said insulating material layer;

characterized in that said control gate region (50a) is physically separated from control gate regions belonging to adjacent stack structures (54) by said protective layer (75);
and in that said word lines (80a) extend on top of said control gate regions (50a) and are in electrical contact with said control gate regions (50a).

14. The device according to Claim 13, characterized by interconnection lines (77, 93, 96) of metal and in that said word lines (80a) comprise metal regions coplanar with said interconnection lines.

15. The device according to Claim 14, characterized in that said interconnection lines (77, 93, 96) and said word lines (80a) are of tungsten.

16. The device according to any of Claims 13-15, characterized in that said stack structures (54) extend on top of a first portion (15) of said substrate (2) and the device comprises diffused source and drain lines (94, 97) extending parallel to and alternating with one another, at a distance, in said substrate (2) between rows of said stack structures (54), said diffused source and drain lines (94, 97) having one end that extends in a second portion (17) of said substrate (2) which is remote from said first portion (15) and being electrically connected to source/drain contacts (92, 95).

17. The device according to any of Claims 13-16, comprising first insulating regions (30a) and second insulating regions (30b) in a first area (15) and, respectively, in a second area (16), separate from said first area (15), of a substrate (2) of semiconductor material, characterized in that said first insulating regions (30a) are formed on top of said substrate (2) and have one first height, and in that said second insulating regions (30b) are formed in trenches (28) extending within said substrate (2) and protrude from said trenches (28) for a second height smaller than said first height.

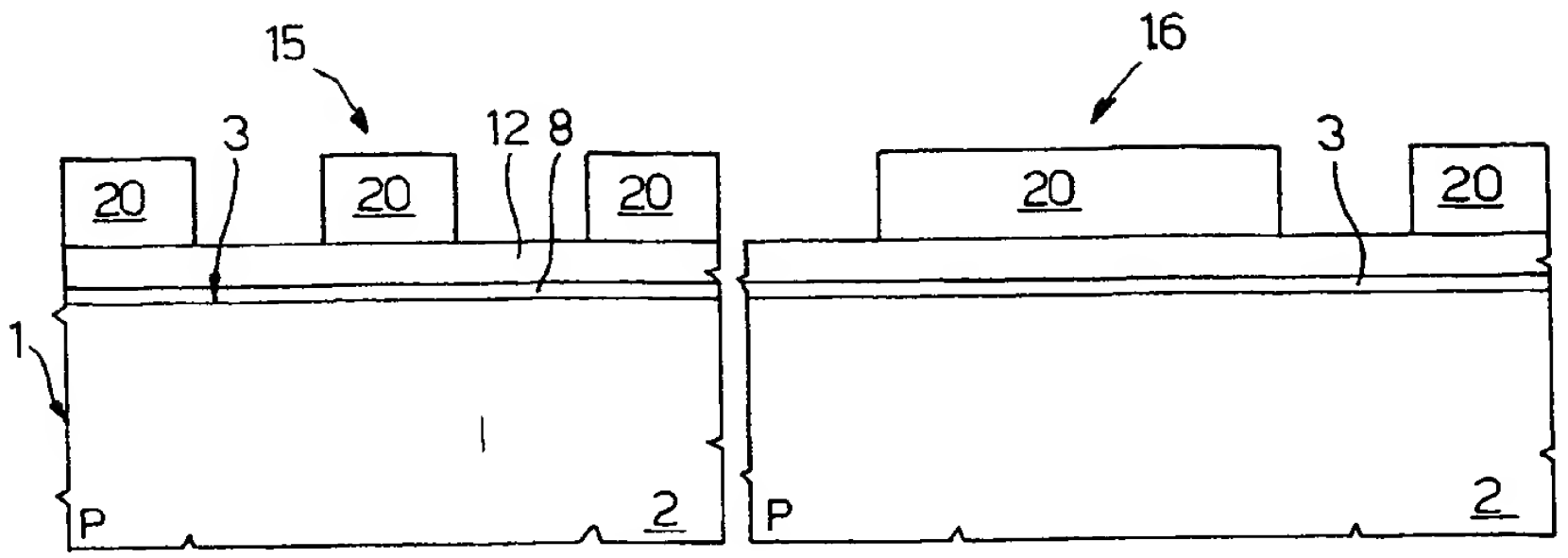


Fig.1

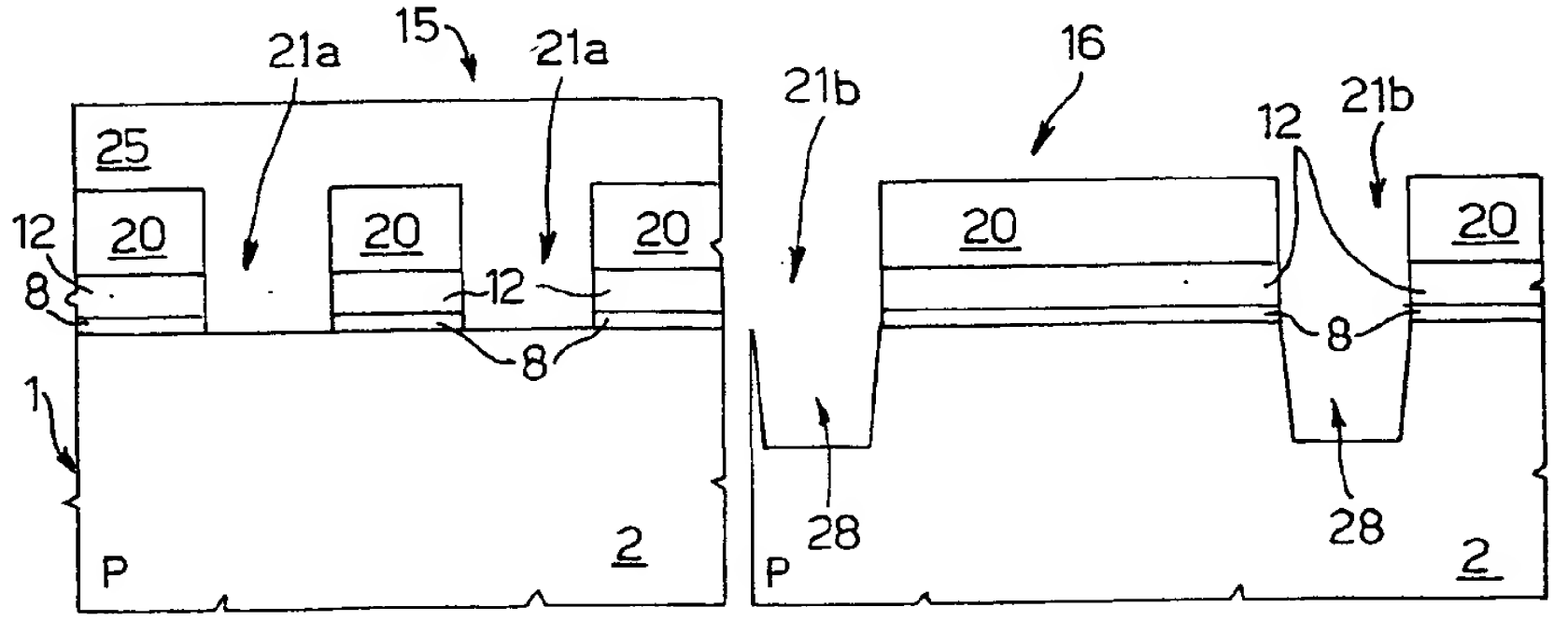


Fig.2

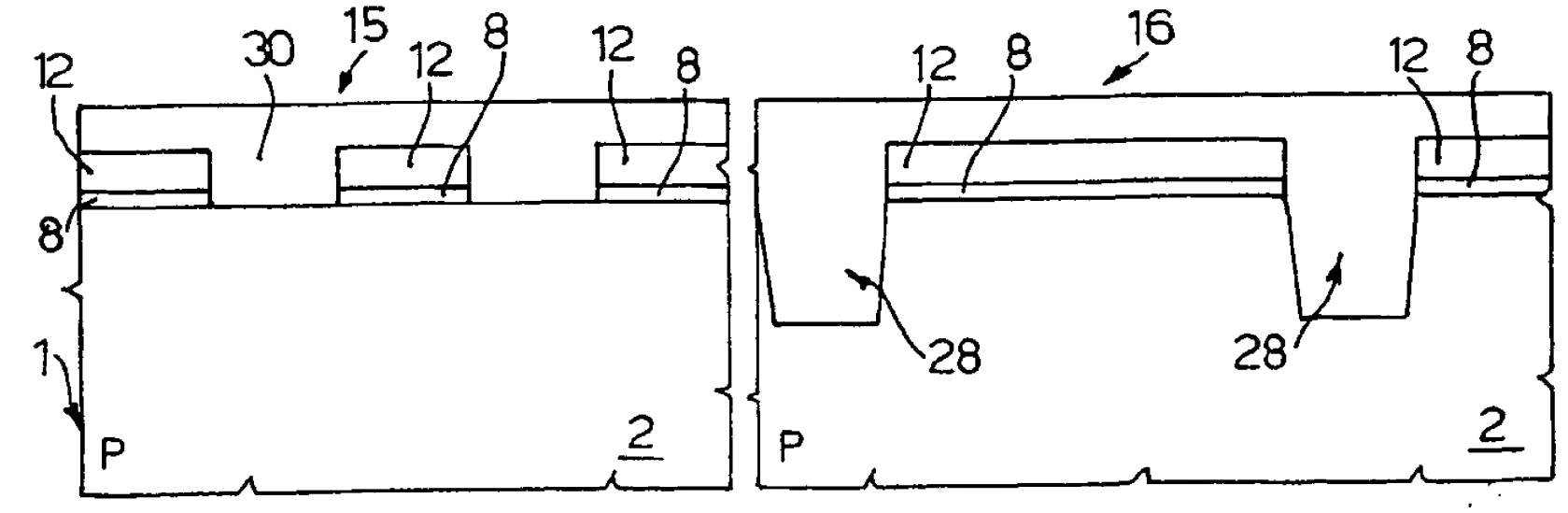
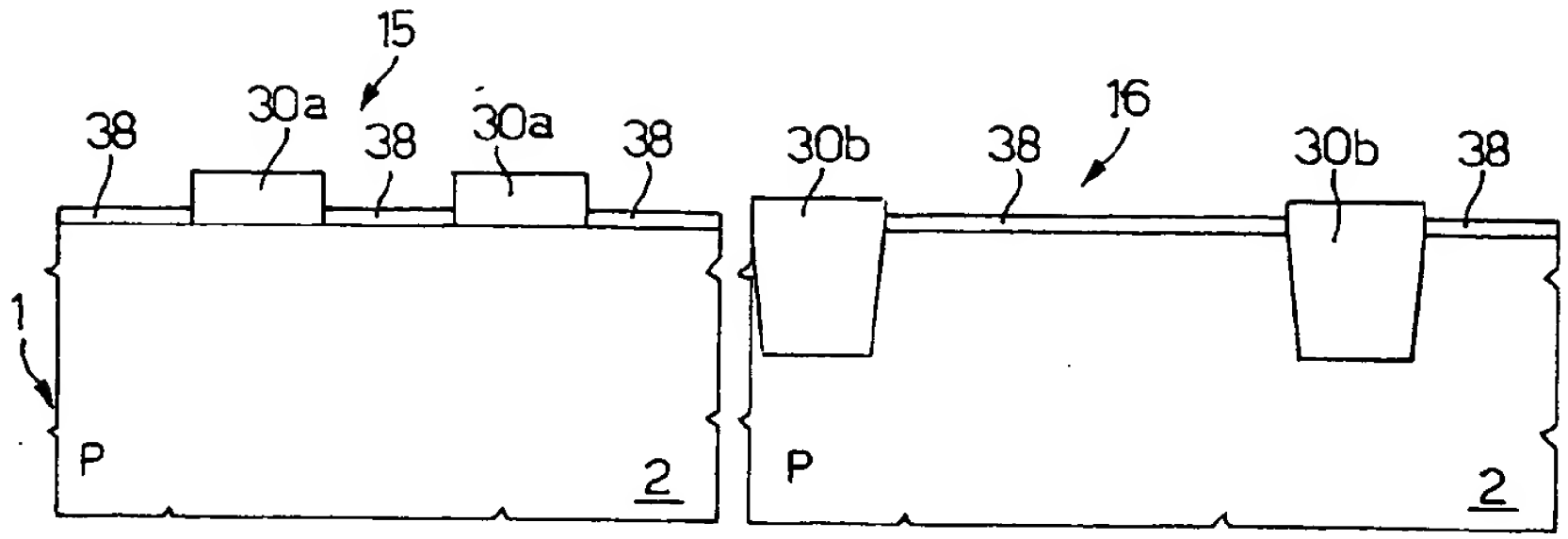


Fig.3



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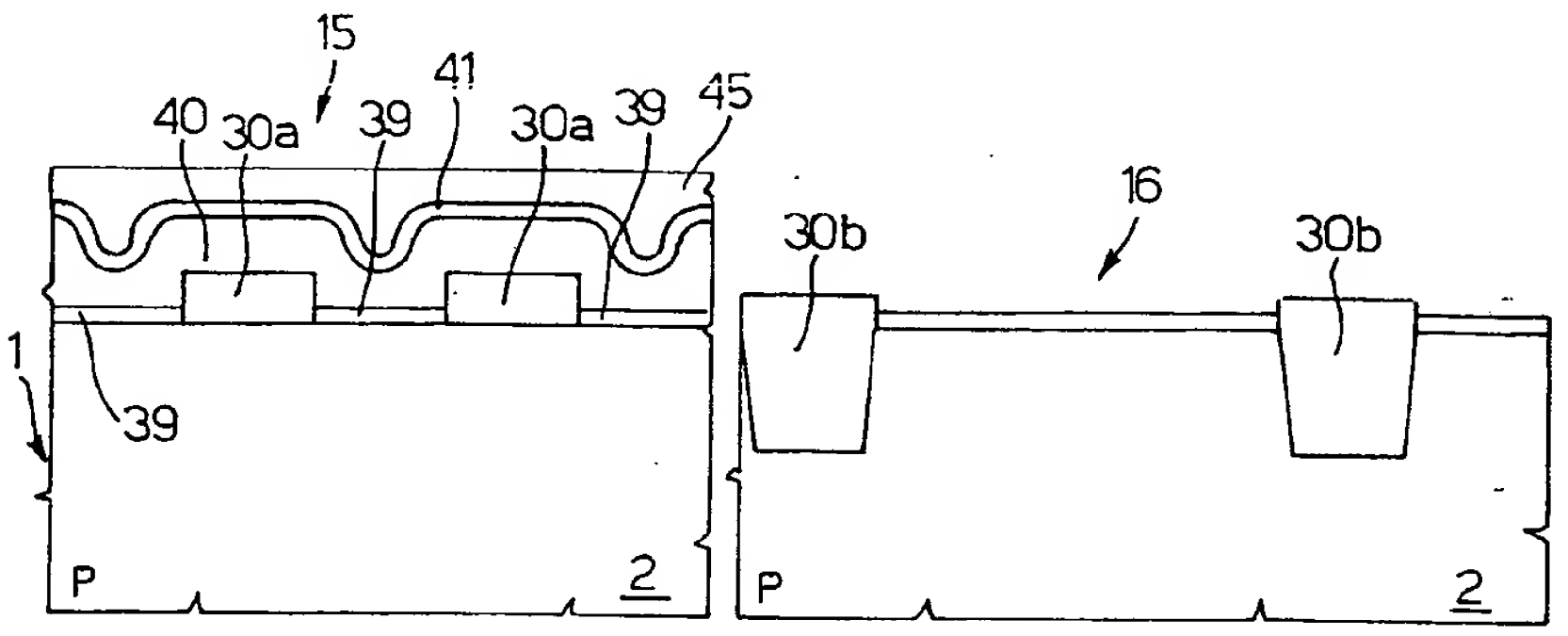

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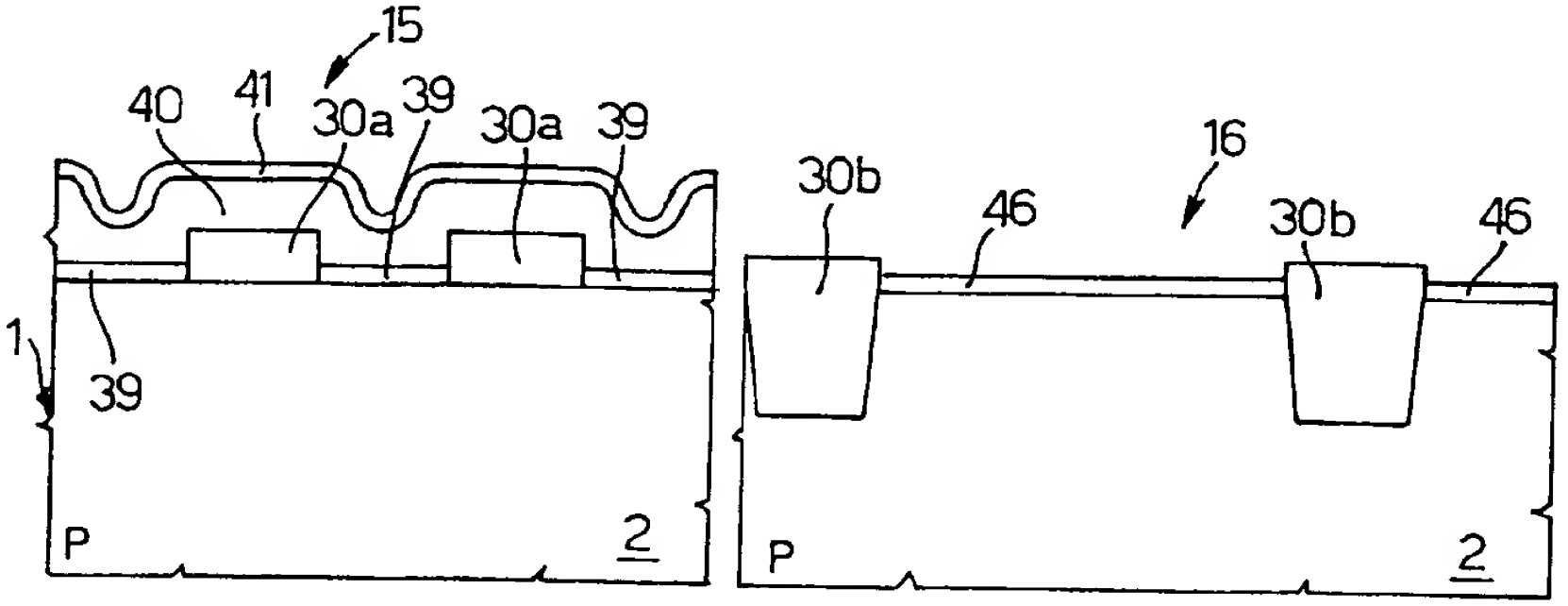

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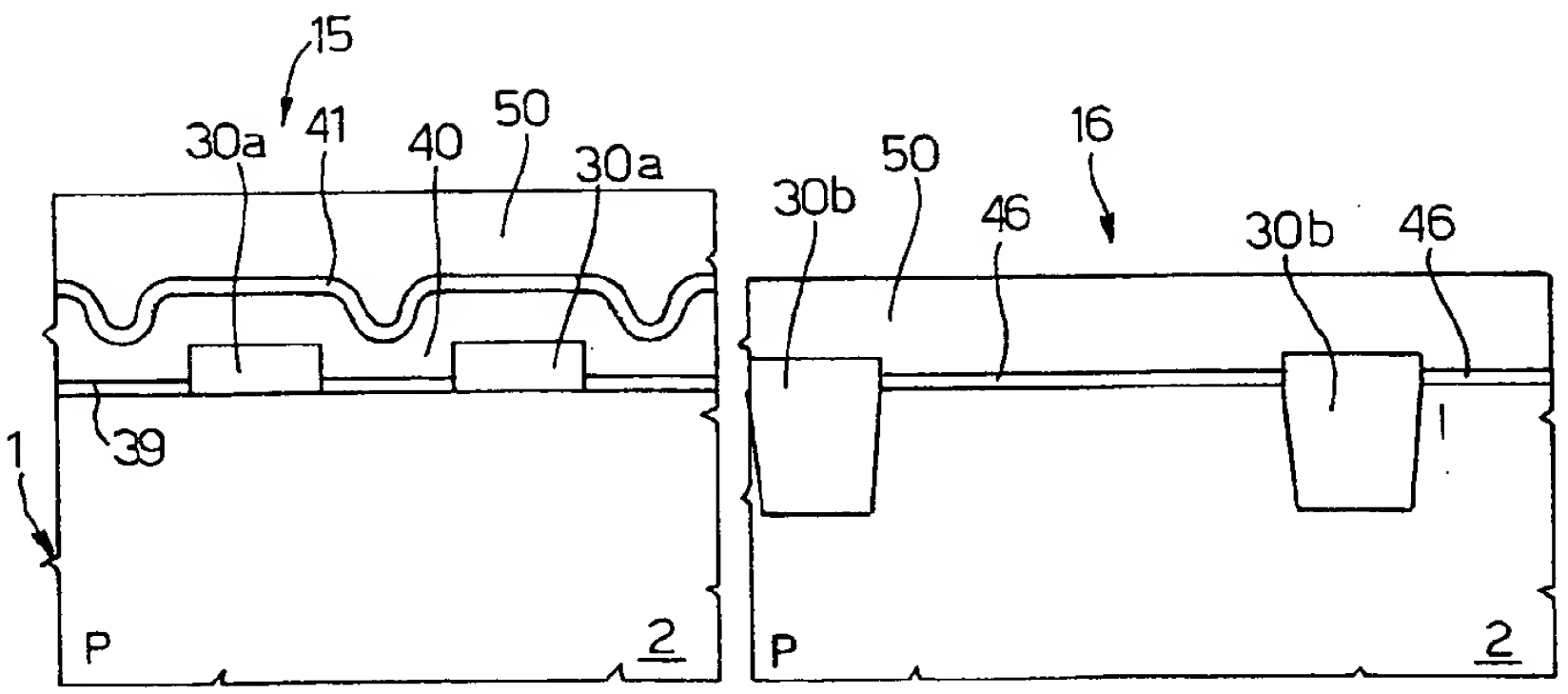

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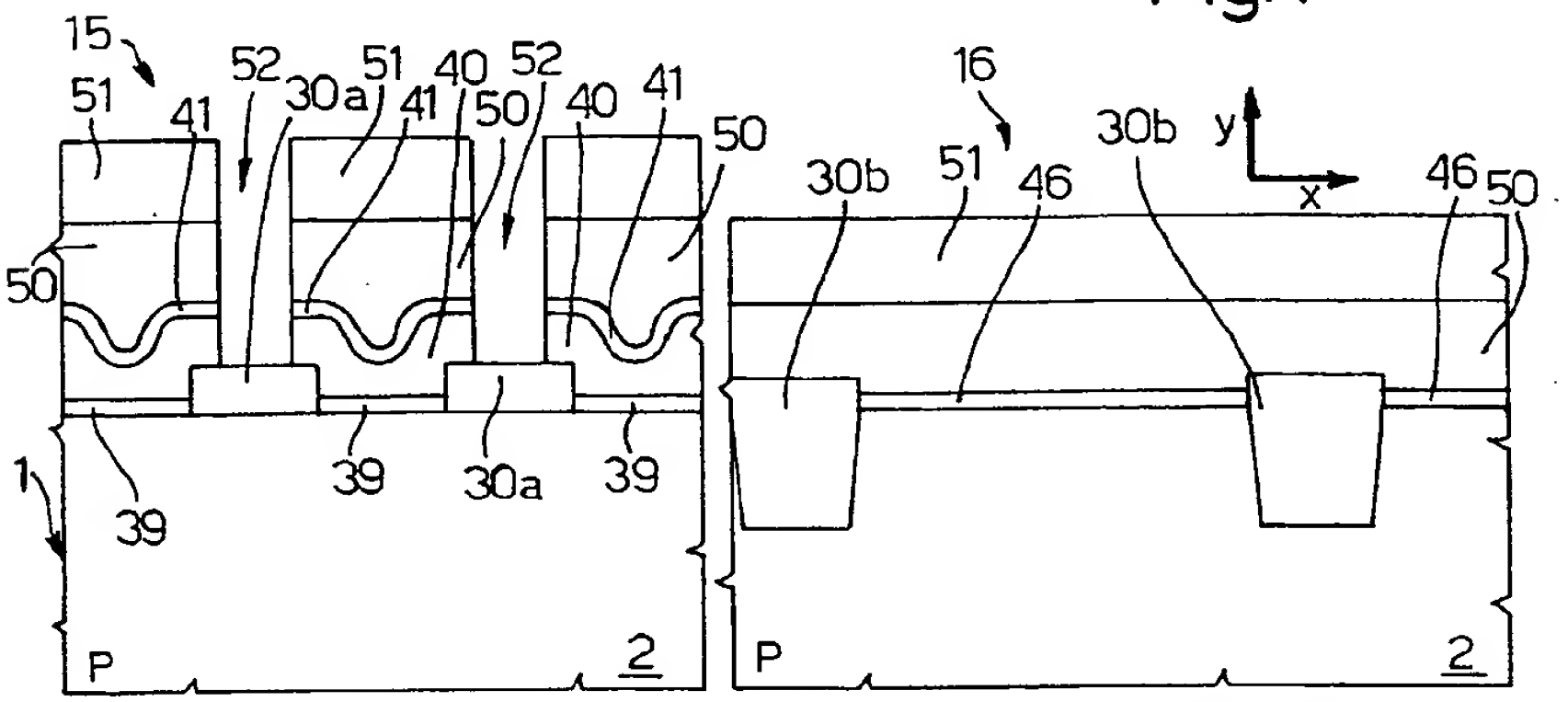

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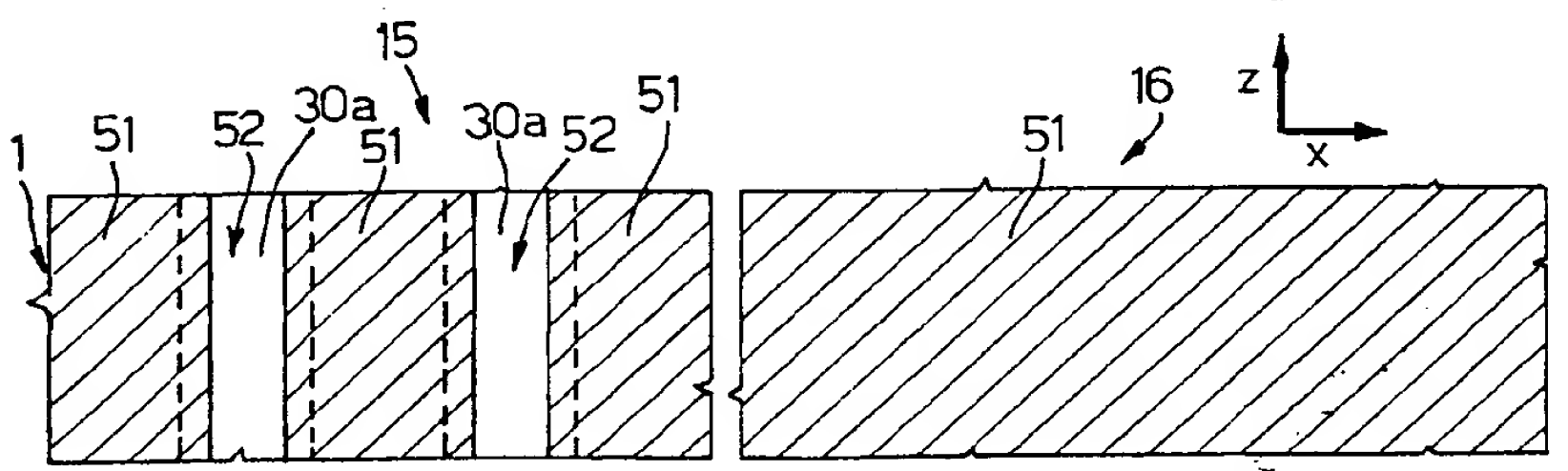

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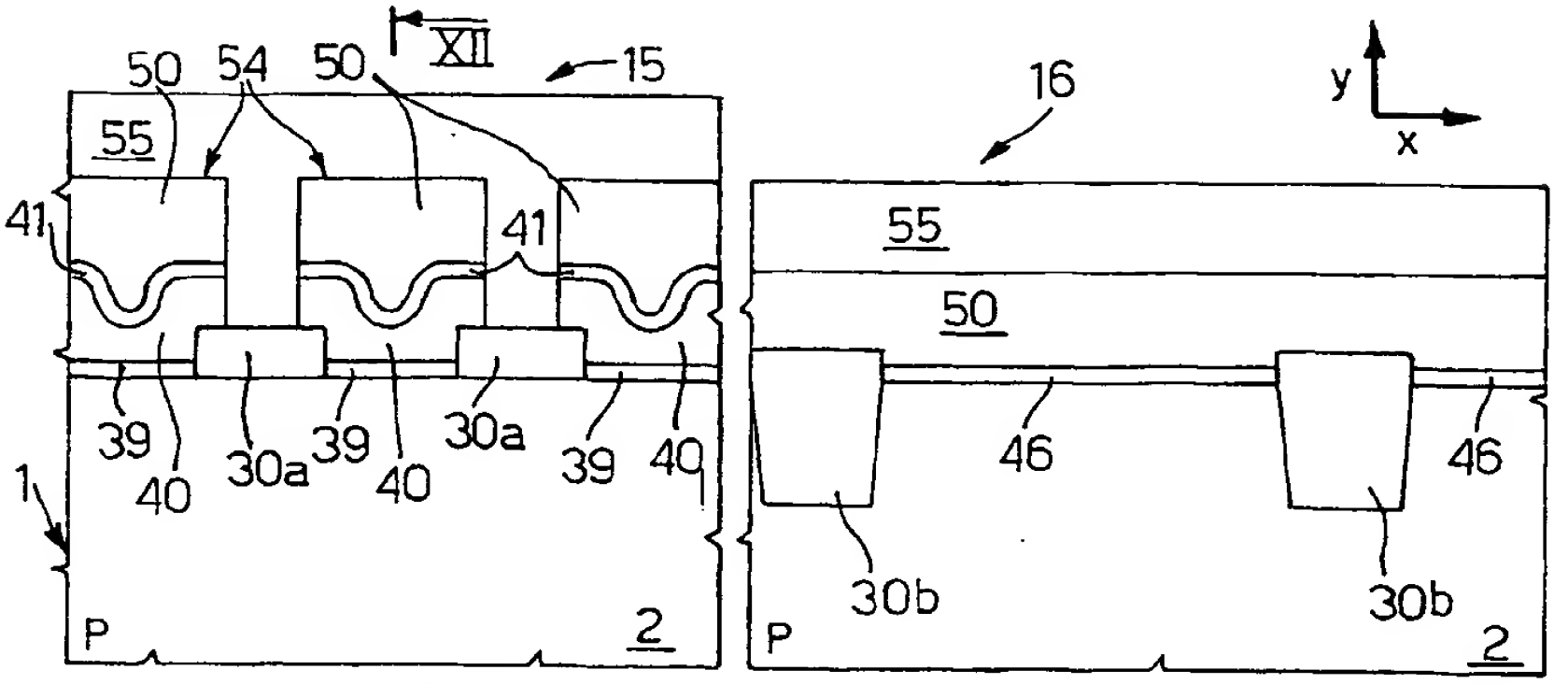

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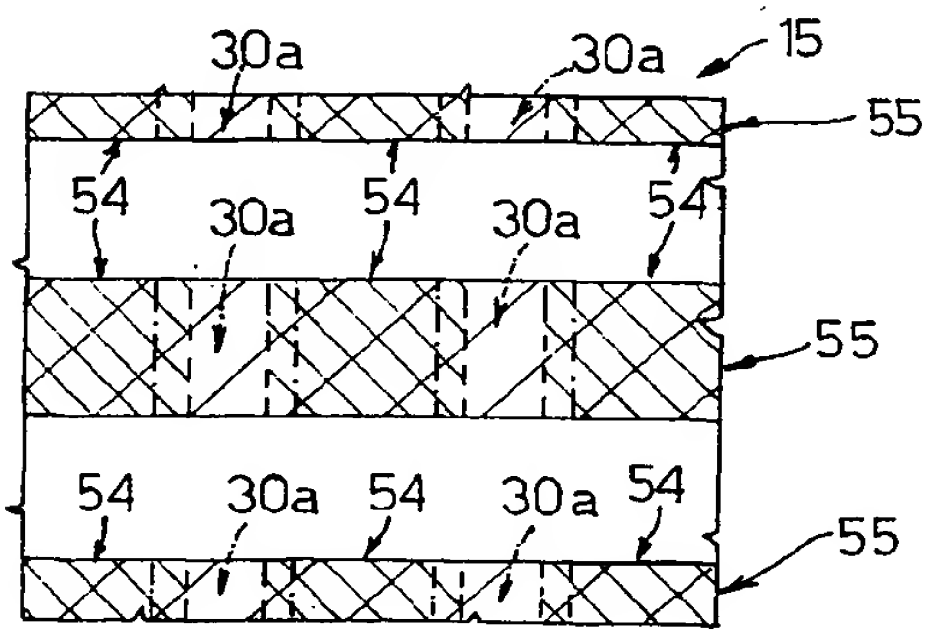

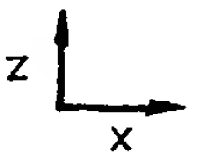

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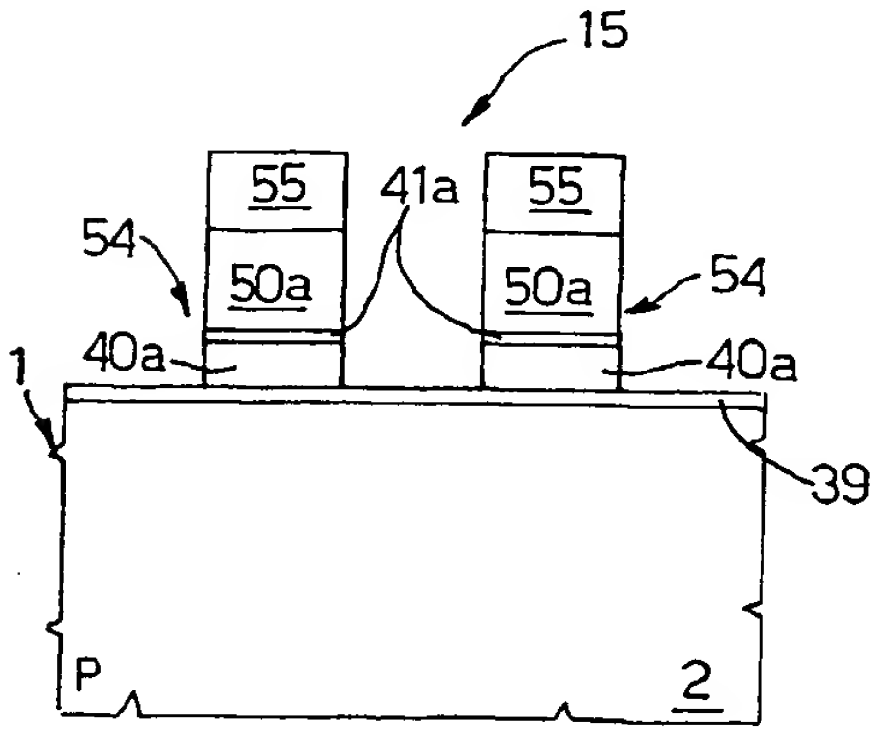

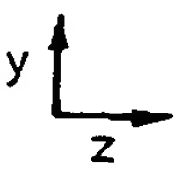

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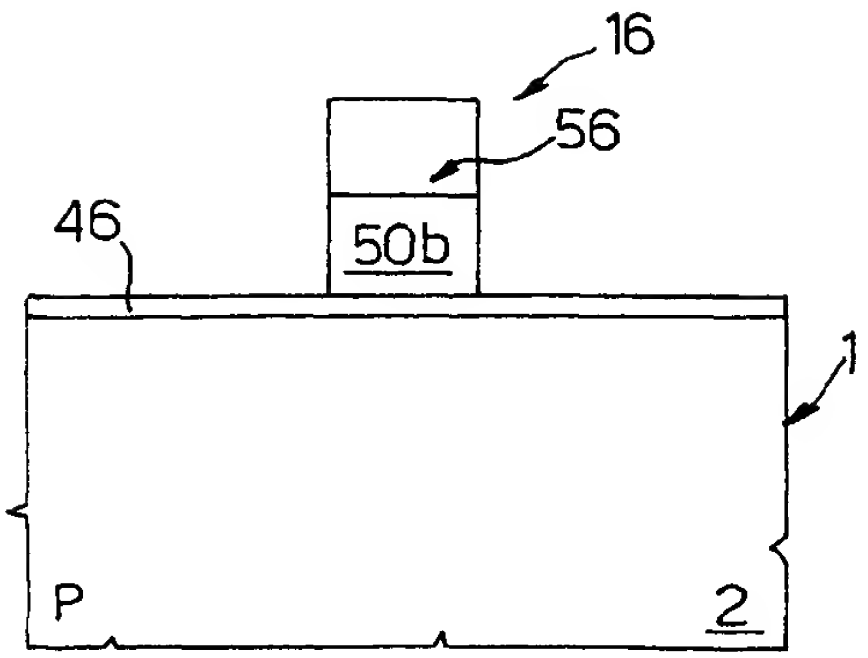


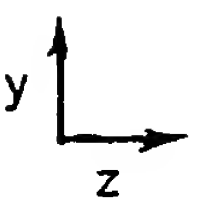
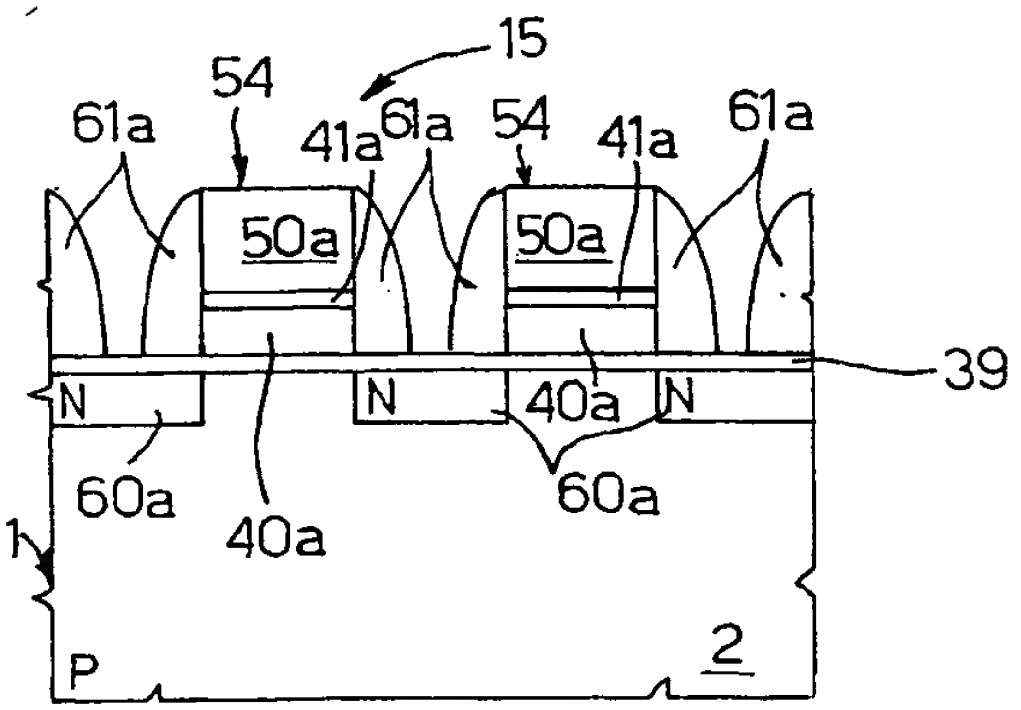
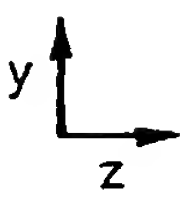


Fig.13





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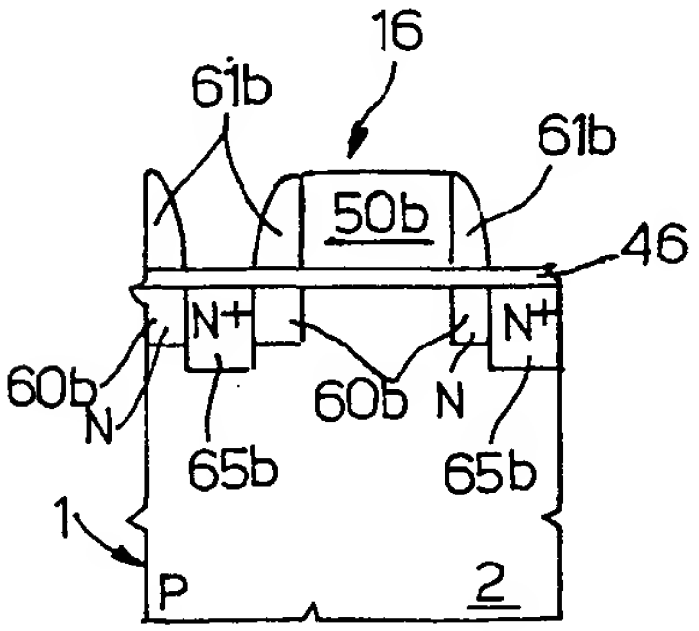

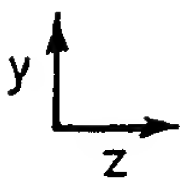

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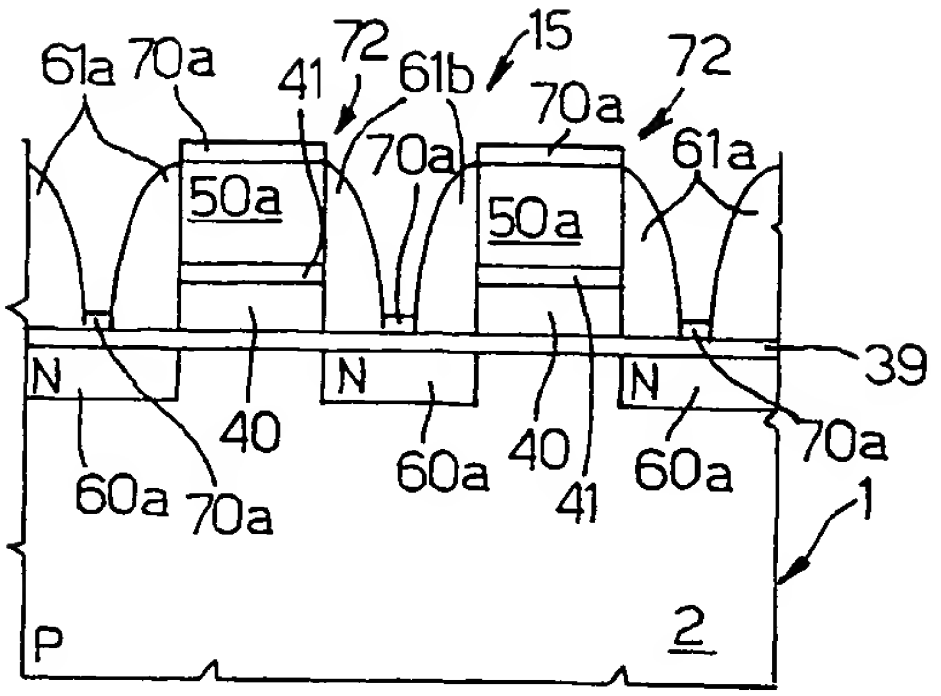

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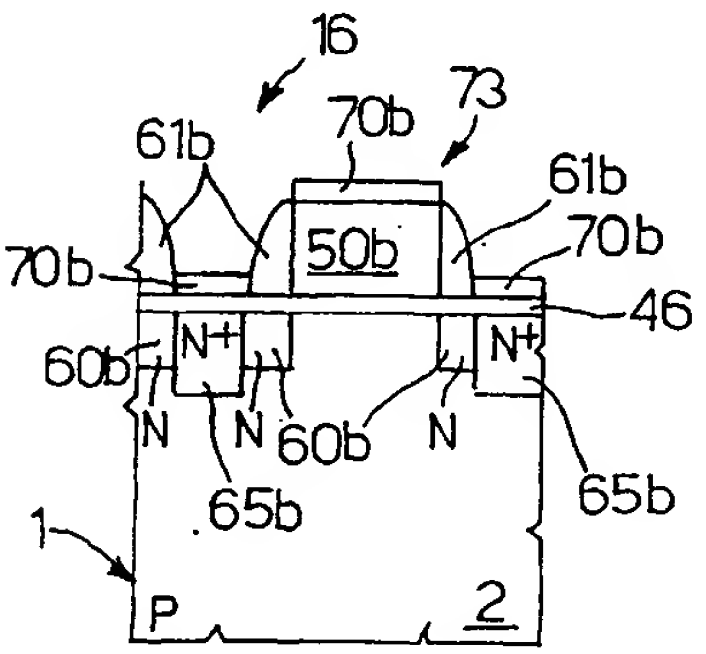

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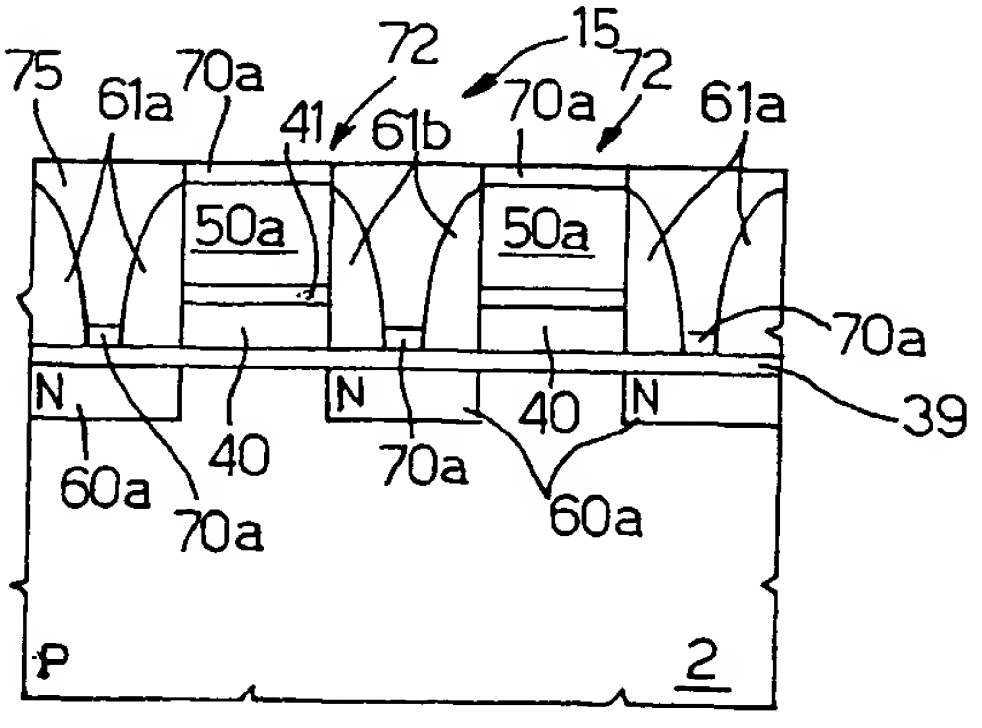

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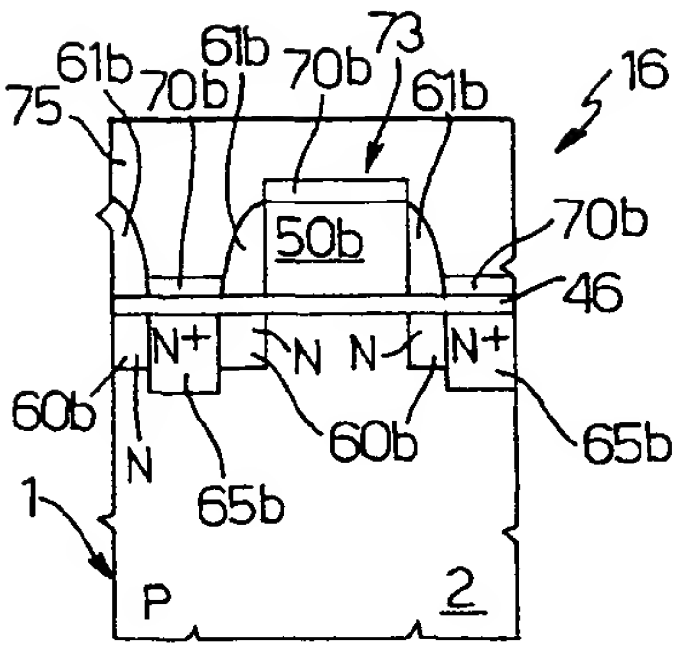

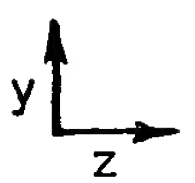

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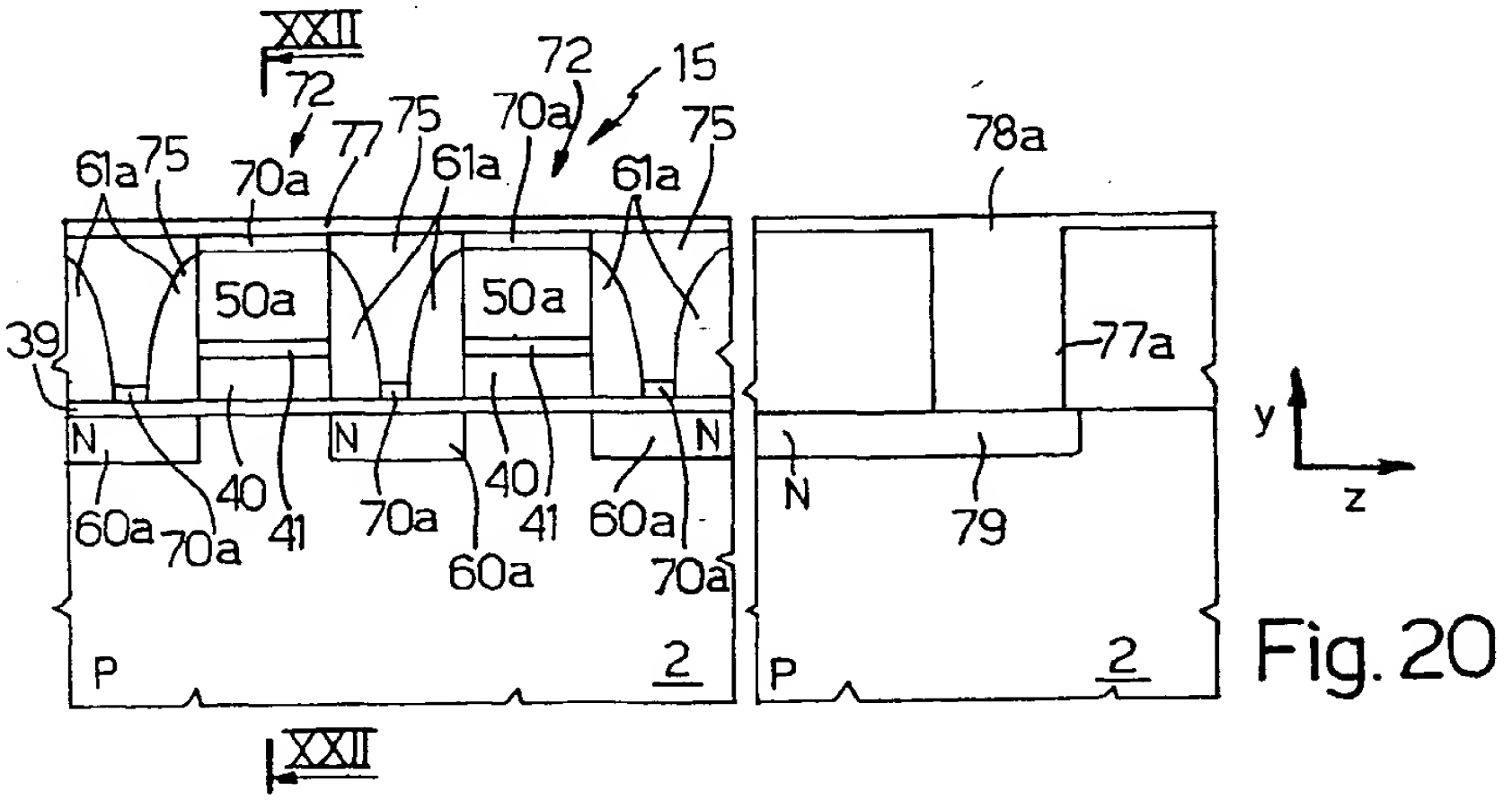

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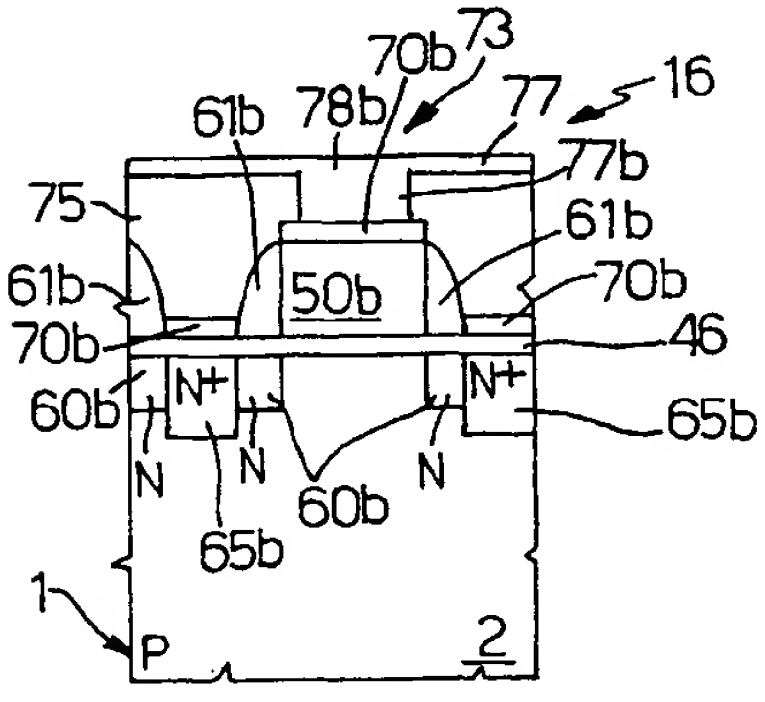

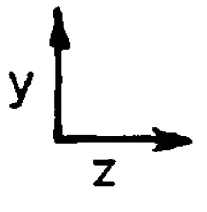

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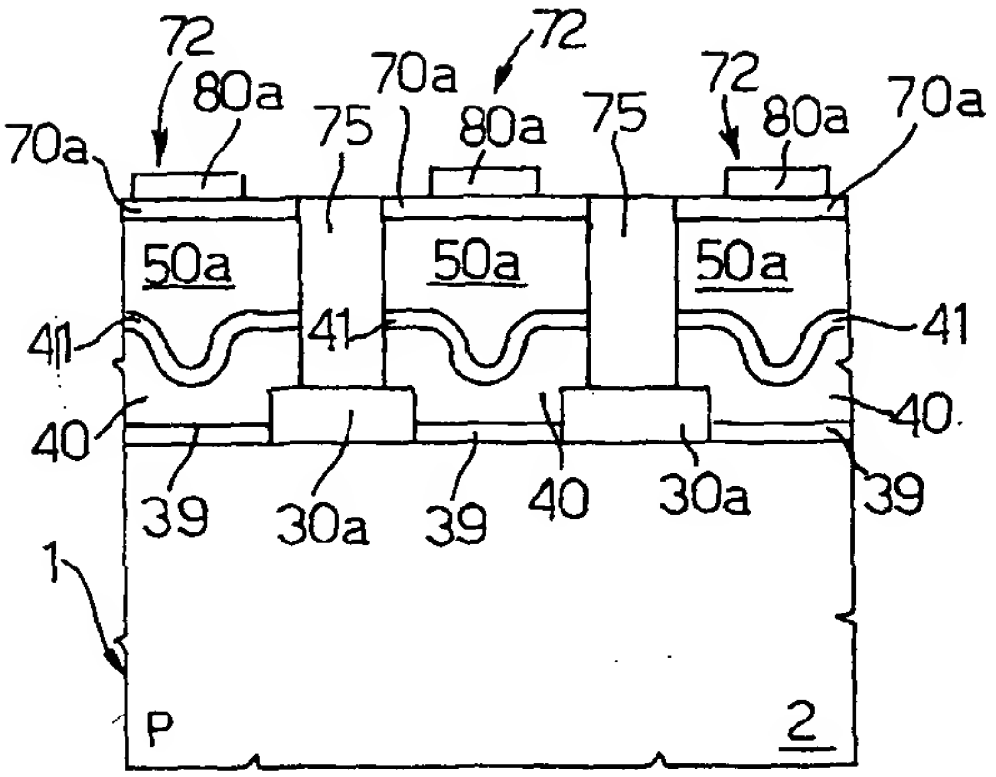

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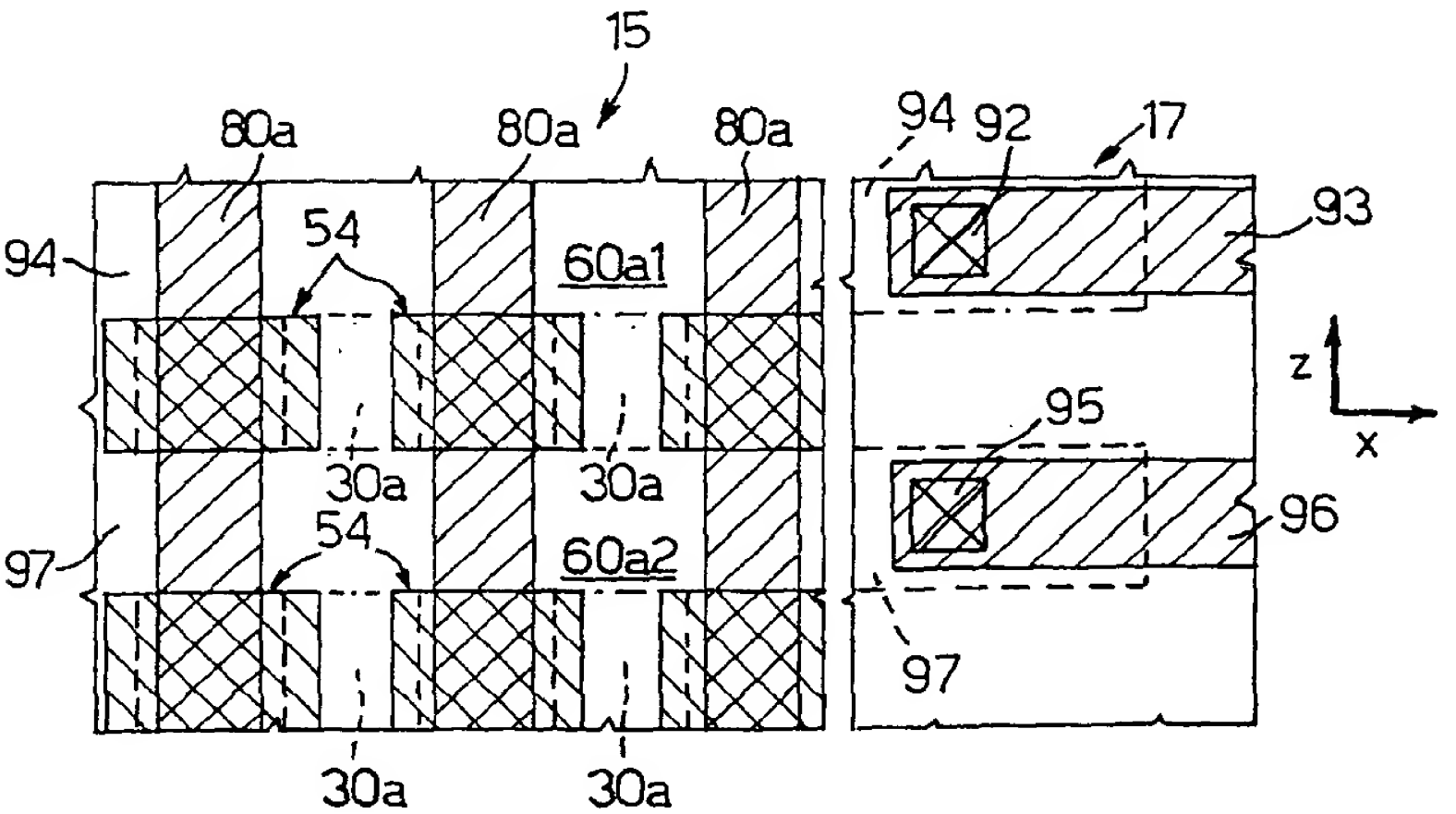

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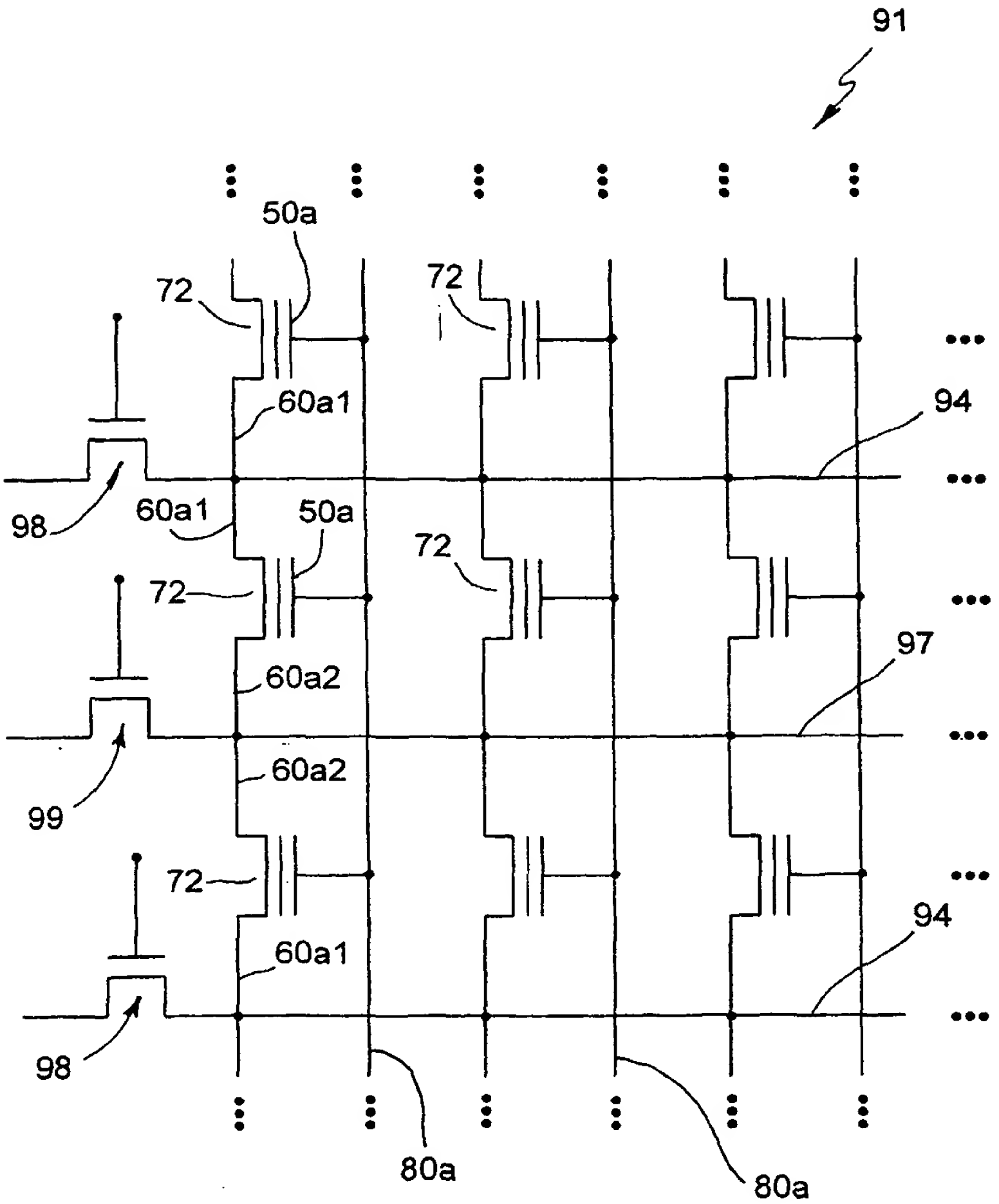

Fig.24

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0735

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	DE 41 13 325 A (INTEL CORP) 31 October 1991 (1991-10-31) * the whole document *	1,2,4-9, 13-16	H01L21/8247 H01L21/8239 H01L27/115
A		3	
X	US 5 200 350 A (GILL MANZUR ET AL) 6 April 1993 (1993-04-06) * the whole document *	1,2,4-9, 13-16	
A	US 5 815 433 A (TAKEUCHI NOBUYOSHI) 29 September 1998 (1998-09-29) * abstract *	1,10-13, 17	
A	WO 94 05037 A (HARRIS CORP) 3 March 1994 (1994-03-03) * abstract *	10,12,17	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12 May 2000	Albrecht, C

EPO FORM 1503 03.82 (P04C01)

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12-05-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 4113325 A	31-10-1991	US 5087584 A	11-02-1992
		FR 2661555 A	31-10-1991
		GB 2243718 A,B	06-11-1991
		JP 4229654 A	19-08-1992
US 5200350 A	06-04-1993	US 5095345 A	10-03-1992
US 5815433 A	29-09-1998	JP 8236646 A	13-09-1996
WO 9405037 A	03-03-1994	US 5382541 A	17-01-1995
		US 5504033 A	02-04-1996

EPO FORM P0459

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